WHAT IS CLAIMED IS:

1. A computer system including a CPU, a memory, and a cache located in a hierarchy class between said CPU and said memory, said computer system comprising:

a coherent controller for determining whether a request supplied from said CPU hits said cache to thereby issue a request to said cache or said memory; and

a cache data controller for controlling reading or writing of data registered in said cache, in accordance with a request issued by said coherent controller;

wherein upon accepting a read request from said CPU, said coherent controller conducts hit decision of said cache, issues an advanced speculative read request to said cache data controller, and issues a read request to said cache data controller if the hit decision is a cache hit.

2. A computer system according to claim 1, wherein said cache data controller comprises:

means responsive to acceptance of an advanced speculative read request issued by said coherent controller, for reading data from said cache and holding the data; and

means responsive to acceptance of a read request and a cache hit decision for sending said held speculative read data to said CPU as response data.

3. A computer system according to claim 1,

wherein if a hit decision is a cache miss, said

coherent controller issues a speculative read data discarding request to said cache data controller, and

wherein upon accepting a speculative read data discarding request issued by said coherent controller, said cache data controller cancels speculative read data of a speculative read request corresponding to the speculative read data discarding request.

4. A computer system according to claim 1, wherein said cache is an n-way associative cache.

5. A computer system according to claim 4, wherein said cache data controller accepts an advanced speculative read request corresponding to n ways issued by said coherent controller, reads out data corresponding to n ways from said cache, and hold the data.

6. A cache data control method in a computer system including a CPU, a memory, and a cache located in a hierarchy class between said CPU and said memory, said cache data control method comprising the steps of:

receiving a request from said CPU;

determining whether said request is an advanced speculative data request;

if said request is a speculative data request,

determining whether a request to the same cache entry as said advanced speculative data request is stored in a speculative read request buffer beforehand; and

if the request is stored in a speculative read request buffer beforehand, disregarding the advanced speculative data request received from said CPU.

7. A cache data control method according to claim 6, wherein if, as a result of determining whether a request to the same cache entry as said advanced speculative data request is stored in a speculative read request buffer beforehand, said advanced speculative data request is not stored in said speculative read request buffer, said method further comprises the steps of:

determining whether said speculative data request buffer is full;

if said speculative data request buffer is not full, registering said advanced speculative data request with an empty entry in said speculative data request buffer;

if said speculative data request buffer is full, invalidating an oldest entry included in said speculative data request buffer; and

registering said advanced speculative read request with said speculative data request buffer.

8. A cache data control method according to claim 6, wherein if, as a result of determining whether said request received from said CPU is an advanced speculative data request, said request is not an advanced speculative data request, but a read request, said method further comprises the steps of:

determining whether an address of the same cache entry as said read request is stored in said speculative read request buffer;

if the address of the same cache entry as said

advanced read request is stored in said speculative read request buffer, reading out data from a pertinent entry of said speculative read request buffer; and

transmitting said data as response data.

9. A cache data control method according to claim 8, wherein if, as a result of determining whether an address of the same cache entry as said read request is stored in said speculative read request buffer, the address is not stored, said method further comprises the steps of:

transferring said read request to said cache;

selecting cache data read out from a pertinent cache entry of said cache; and

transmitting said cache data as response data.

10. A cache data control method according to claim 6, wherein if, as a result of determining whether said request received from said CPU is an advanced speculative data request, said request is not an advanced speculative data request, but a write request, said method further comprises the steps of:

determining whether an address of the same cache entry as said write request is stored in said speculative read request buffer;

if the address of the same cache entry as said write request is stored in said speculative read request buffer, invalidating a pertinent entry of said speculative request buffer;

transmitting said write request to a data

section of said cache; and

writes said write request into a specified entry of said cache data section.

11. A cache data control method in a computer system including a CPU, a memory, and a cache located in a hierarchy class between said CPU and said memory, said cache data control method comprising the steps of:

receiving a memory access request from said CPU;

determining whether said memory access request is a read request;

if said memory access request is a read request, issuing an advanced speculative read request to a cache data controller, and sending a cache entry number of said read request to a cache tag section;

reading out a cache tag of said cache entry number from said cache tag section;

determining whether said cache tag read out hits a cache tag of said read request; and

upon a hit, issuing a read request to said cache controller.

12. A cache data control method according to claim 11, wherein if a cache miss occurs between the cache tag read out from said cache tag section and the cache tag of said read request, said cache data control method further comprises the steps of:

issuing a read request; and

registering the cache tag of said memory access

request with said cache tag section.

13. A cache data control method according to claim 11, wherein if the request received from the CPU is a write request, said cache data control method further comprises the steps of:

reading a cache tag from said cache tag section and determining whether a cache hit has occurred;

if as a result of said determination a cache hit has occurred, issuing a write request to said cache data controller; and

sending write data from a data buffer to said cache data controller.

14. A cache data control method according to claim 13, wherein if the determination on the cache tag read out from said cache tag section results in a cache miss, said cache data control method further comprises the steps of:

issuing a write request; and

sending write data from the data buffer to said memory.

15. A computer system according claim 1, wherein said cache is a set associative cache.

16. A cache data control method according to claim 6, wherein a set associative cache is used as said cache.

17. A cache data control method in a computer system including a CPU, a storage controller, a cache tag section connected to said storage controller, a cache data section, and a cache data controller connected

between said cache data section and said storage controller, said cache data control method comprising the steps of:

reading cache data from said cache data section to hold in said cache data controller in response to a first read request from said storage controller; and

sending said cache data from said cache data controller to said storage controller in response to a second read request issued from said storage controller based on cache hit result from said cache tag section.

18. A cache data control method according to claim 17, further comprising a step of including a bit indicating whether a request issued from said storage controller is either one of said first and second data requests.